IN THE SPECIFICATION:

Please replace paragraph [0007] with the following amended paragraph:

[0007] Shared-memory multiprocessor systems present special issues regarding cache implementations and management. In shared-memory multiprocessor systems, all processors can access all memory including main and cache memory. This enables the tasks on all of the processors to efficiently and easily share data with one another. However, this sharing must be controlled to have predictable results. Conventionally, [[share-]]shared memory multiprocessor systems have hardware that maintains cache coherence and provides software instructions that can be used to control which processor is writing to a particular memory location. In order to prevent multiple processors from storing to the same memory location (or cache line) at the same time, most shared memory multi-processors use a snoop-invalidate cache protocol to allow a processor to write data to a memory location (or cache line) only if it has an exclusive copy of the cache line containing the memory location.

Please replace paragraph [0032] with the following amended paragraph:

[0032] The method for purging and updating cache lines comprises a state called "temporarily invalid" that may be entered into the state field 208 of the cache directory 200. Illustratively, the temporarily invalid state indicates that the cache line 202 once held the memory location indicated by the tag 204 but is currently being accessed exclusively by another processor that requested the cache line 202 exclusively. While the cache line 202 is in a temporarily invalid state, the cache line will not be overwritten by a new cache entry. A new cache entry will first replace a cache line that is in an invalid state. If no cache lines are in an invalid state, the new cache entry will replace the oldest cache line 202 as indicated by the historical information contained in the replacement information 206. The temporarily invalid cache line will only be overwritten if the replacement information 206 indicates that the temporarily invalid cache line is the oldest cache line.

Please replace paragraph [0038] with the following amended paragraph:

[0038] For instance, assume a first processor executes a store instruction to put data 1234H to memory address [56789H] (square brackets indicate the enclosed number is a memory address). Assume further it is known that a second processor will soon reads data from memory address [56789H]. To improve the performance of the second processor, the first processor may execute an instruction 128 after the first processor executes the store instruction. For the instruction 128, field "RB" 312 can hold the processor number of the second processor. Field "M" 304 can be 0 so that the second processor whose processor number is in field "RB" 312 is selected to be updated. Field "P" 306 can be 1 so that only the second processor is selected to be updated. Field "H" 308 can be 0 so that an L1 cache of the second processor is updated.